Digital sync-tip clamping: a new approach to video-signal conditioning

LAZAR SHIFRIN, ADVANCED IMAGING SOLUTIONS

Digital sync-tip clamping allows an ac-coupled ADC to digitize analog video without restoring the horizontal timing. You can implement the technique as a stand-alone clamping ADC or as a complete front-end configuration, including sync detection and AGC.

In digital sync-tip clamping, a stand-alone "clamping" ADC (CADC) incorporates the dc-restore function at its input and eliminates the need for external timing strobes. This technique encompasses a complete front-end architecture, including sync detection and automatic gain control (AGC) and provides more system-design flexibility in video applications than conventional ADCs. This CADC architecture is a promising configuration for a single-chip video-conditioning front end.

The two main advantages of digital sync-tip clamping are high accuracy and asynchronous operation. In other words, with a CADC, you don't need to recover the horizontal timing of the analog video. This feature simplifies the design if the application specifies a $4F_{SC}$ sampling rate, such as in comb filters, or uses a free-running sample clock. (The F_{SC}, or subcarrier frequency, for NTSC video is 3.58 MHz.)

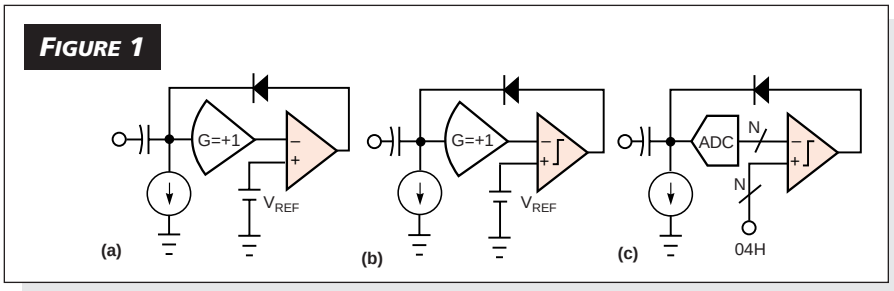
With a conventional back-porch clamp, dc restoration, or clamping, must occur before you set the signal level at the ADC's input. However, to digitally extract timing-control signals, the circuit needs to first define either the sync-tip or the back-porch reference-voltage levels. To break this "loop," the circuit must initialize the digital timing with an auxiliary analog separator. The CADC avoids this problem. Because the digitized video has a fixed dc level, you can directly obtain the sync information and the AGC's error signal from the digital data.

Video front end needs clamping

To digitize an ac-coupled video waveform, dc restoration is necessary to put a dc component back into the video signal. Usually, some type of switchable device, such as an analog switch, operational transconductance amplifier (OTA), or S/H amplifier, performs the dc restoration function. The circuitry adjusts the clamp level to the chosen value during the back-porch section of the video signal. Then, the circuitry stores this value during the active-line time. It is important to set the clamp level during a specific line interval because the circuit needs to recover the horizontal timing information before clamping. In other words, the circuit must recover the information from the ac-coupled signal.

Another dc-restoration method based on sync-tip clamping uses no temporal information. This essentially analog technique is subject to temperature dependencies and part tolerances; therefore, it is too precise for dc restoration. However, designers often use this technique for sync detection. **Figure 1a** shows the sync-tip clamp used in such ICs as the industry-standard LM1881 (National Semiconductor, www.nsc.com), the EL4581/83 (Elantec, www.elantec.com), the GS4881 and GS4991 (Gennum Corp, www.gennum.com), and others. This circuitry clamps the negative-going sync tip to the V_{REF} voltage. A unity-gain buffer outputs the clamped video.

FIGURE 1



Sync-tip clamping using either an op amp (a) or a comparator (b) is a common technique for sync detection. Digital sync-tip clamping (c) embeds an ac-coupled ADC in the clamping feedback loop, a scheme that performs dc restoration without horizontal-timing information.